# PERFORMANCE EVALUATION FOR AN NOC ARCHITECTURE

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*Course: QH-2007-I/CQ, Major: Electronics - Communications*

**Abstract**

Nowadays, with the evolution of semiconductor technology, we can integrate more and more IP (Intellectual Properties) cores into a system to meet the high demand of applications. This increases the on-chip communication load, especially in the large, complex systems. Network-on-Chip (NoC) paradigm has been proposed and quickly known as the next paradigm of System-on-Chip (SoC) to response to on-chip communication problems. In this trend, VLSI system design group at the University of Engineering and Technology, VNU Hanoi has also developed a 2D-mesh NoC architecture. However, to bring this architecture into real application systems, we have to evaluate the performance of the designed NoC architecture.

As presented in literature, different NoC architectures provide different performances. So that, the performance evaluation helps us to decide the main parameters for designing our own NoC architecture such as topology, commutation modes, buffer strategy, routing algorithm and others. Currently, some works have been proposed in regarding to performance evaluation. From the 2D-mesh NoC architecture developed at the group, this thesis studies about NoC architectures and presents a performance evaluation model for the 2D-mesh NoC architecture. However, the method can be modified to be used for evaluating other NoC architectures.

The thesis is organized as follows: Chapter 1 briefly introduces to NoC paradigm and basic definitions, especially the 2D-mesh NoC architecture developed by VLSI System Design group. This architecture is used in the proposed evaluation model. Chapter 2 presents several concepts related to the performance of an NoC architecture and the previous works related to performance evaluation. Chapter 3 is presented the proposed performance evaluation model for 2D-mesh NoC architecture. Finally, experimental results and conclusion will be given in Chapter 4.

**Keywords**: Network-on-Chip, Performance evaluation, System-on-Chip,