DESIGN AND MANUFACTURE THE SIGNAL RECEIVER - FREQUENCY 915MHZ USING CHIP SA620DK

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Abstract:

Thesis focuses on research, design, manufacture a receivers operating at frequencies of 915MHz. My thesis includes three chapters.

Chapter 1 and chapter 2 present the basic theory of the general receiver and the receiver using chip SA620DK particular. Chapter 1 proposes an overview of the receiver, the basic parameters of the receiver such as sensitivity, selectivity, repeat news quality..., and operation principle analysis of the receiver including the principles of the blocks: low noise amplifier (LNA), voltage controlled oscillator (VCO) and frequency mixer (MIXER). Chapter 2 focuses on analysis of the blocks structure within the chip SA620DK.

Chapter 3 is practical. This chapter designs the receiver basing on characteristics, principles of the blocks of the chip SA620DK presented in previous chapters. After that, the product is tested, measured and assessed its quality. From the results of measurement, author optimizes the receiver.

The conclusion section summaries the subject, shows the parts which have been done and the parts lacking in the thesis, and then proposing future development.

Keywords: *915MHZ, Receiver, SA620DK*